etchstop material layer underlying the trenches until the thin inorganic dielectric layer is reached;

(n) filling the vias in the via level organic dielectric layer and the thin inorganic dielectric layer, and trenches in the organic dielectric etchstop layer and metal level inorganic dielectric layer with a metal.

20. (Amended) The integrated circuit structure [process] of claim 15 wherein steps (b) through (n) are repeated at least once on the previously formed integrated circuit structure.

Please cancel claims 9-10, 13-14, 17-18, 21-22 without prejudice and subject to applicant's right to file a divisional application for this subject matter.

REMARKS

A new drawing Figure 2 is enclosed.

The Examiner has subjected this application to restriction under 35 U.S.C. 121. The Examiner has formed two groups of claims, Group I for claims 1-6, 9-10, 13-14, 17-18 and 21-31 drawn to a device and Group II for claims 7-8, 11-12, 15-16 and 19-20 drawn to a process. The Examiner has asserted that these groups of claims represent distinct inventions and may properly be restricted. Applicants hereby elect claim Group I for claims 1-6, 9-10, 13-14, 17-18 and 21-31 for examination. The above amendment re-states the claims in the format of the elected invnetion. Applicants reverve the right to

file a divisional application for the process claims.

Respectfully submitted,

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Date: November 21, 2000

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage pre-paid in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on November 21, 2000.

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Figure 2 Multi-Level Interconnection Architecture II